What is claimed is:

1. A semiconductor memory device, comprising:

a memory cell group comprising a plurality of memory cells arranged in a matrix;

specification means for specifying sequentially memory cells addressed by consecutive addresses in the memory cells, and for entering them in an active state;

data input-output (I/0) means for performing a data read-out/write-in operation (data I/0 operation) for the consecutive memory cells specified by the specification means under a control based on a read-out/write-in signal provided from an external section;

count means for counting the number of cycles of a basic clock signal provided from an external section; and

control means for receiving at least one or more specification signals provided from an external section,

for outputting a control signal per specification signal for specifying a particular cycle as a starting cycle to count the number of the cycles of the basic clock signal, and

for instructing the count means to count the number of counts of the basic clock signal based on the control signal, and for controlling a specification operation executed by the specification means and the data I/0 operation of the data I/0 means, so that the memory access operations for the memory cell group are controlled.